AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

Page 2, paragraph 2:

The DRAM 50 receives a plurality of control signals CTL and a plurality (only two bits shown in Fig. [[2]] 1) of external address signals ADD via external terminals. The control signals CTL include a chip enable signal /CE, a write enable signal /WE, and an output enable signal /OE. The external address signals ADD include address signals A0 and A1. The signals /CE, /WE, /OE, A0, and A1 are input to a transition detection signal generation circuit 70 via input buffers 61, 62, 63, 64, and 65, respectively. The input buffers 61 to 65 function as initial input stage circuits, which convert an input signal to a signal having a level corresponding to the internal voltage of the device. Further, the input buffers 61 to 65 are each configured by a CMOS inverter or a C/M differential amplifier.

Page 15, paragraph 7:

Fig. 7 is a waveform chart illustrating an example of a deficient mode of the semiconductor memory device of Fig. [[8]] 1;

Page 31, paragraph 4:

The transition detection signals mtdcs and mtdrs are generated when the chip enable signal /CE goes low, and the refresh start signal ref-start is generated (refresh operation is started) in accordance with the refresh transition detection signal mtdrs. When the refresh operation ends, the read/write start signal rw-start (more specifically, write start signal) is generated in accordance with the command transition detection

signal mtdcs, which is generated when the chip enable signal /CE goes low, to start the write operation.